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FREQUENCY AND TEMPERATURE TESTS FOR LATERAL NONUNIFORMITIES IN MIS CAPACITORS

C. C. Chang and Walter C. Johnson

PRINCETON UNIVERSITY
Department of Electrical Engineering
Princeton, New Jersey 08540
Principal Investigator: Walter C. Johnson
Telephone: (609) 452-4621

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Two techniques are presented for distinguishing between lateral nonuniformities and interface states in metal-insulator-semiconductor capacitors, one based on the frequency dependence of the response of interface states and the other on the freeze-in of carriers in interface states at liquid nitrogen temperature. Experimental examples are given of the use of both techniques.

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FREQUENCY AND TEMPERATURE TESTS FOR LATERAL NONUNIFORMITIES IN MIS CAPACITORS

C. C. CHANG
Industrial Technical Research Institute
Hsinchu, Taiwan

and

WALTER C. JOHNSON
Department of Electrical Engineering
and Computer Science
Princeton University
Princeton, New Jersey 08540

ABSTRACT

Interface states and lateral nonuniformities produce very similar abnormalities in the C-V curves of MIS capacitors. Two C-V techniques are presented here for distinguishing between them. The first technique is based on the frequency dependence of the interface-state capacitance, and utilizes the resulting frequency dispersion of the "high-frequency" capacitance in the depletion regime, which occurs in a frequency range typically between a few hundred Hz and 1 MHz. The second method utilizes a freeze-in of carriers in the interface states at liquid nitrogen temperature. A sweep of bias from accumulation into deep depletion at low temperature produces a C-V characteristic which, when compared with the corresponding ideal characteristic, reveals the presence of lateral nonuniformities. A complementary test is provided by temporary illumination of the deep-depleted structure followed by a sweep of bias from inversion into accumulation. A ledge in the C-V characteristic reveals the presence of interface states in the central half of the bandgap.

I. INTRODUCTION

A frequently observed abnormality in the capacitance-voltage (C-V) curves of metal-insulator-semiconductor (MIS) capacitors is a stretch-out of both the low-frequency (quasi-static) and high-frequency C-V curves along the voltage axis, accompanied by abnormally large values of low-frequency capacitance in the region that would correspond to the depletion regime in a uniform MIS capacitor. It is well recognized that these anomalies can arise from either of two completely different sources: (1) electronic states at the insulator-semiconductor interface, or (2) lateral nonunformities in the MIS structure, for example nonuniform insulator thickness, laterally nonuniform substrate doping, or, most commonly, nonuniform charge storage in the insulator [1],[2]. In many circumstances, such as in studies of radiation damage or the effects of high-field stressing, it is important to be able to identify the cause of C-V stretch-out and to characterize the effect correctly.

When an MIS structure is laterally uniform and any C-V stretch-out is therefore caused only by interface states, the density of interface states as a function of energy can be obtained by any one of a number of well known and effective methods [3-8]. The situation regarding the identification and characterization of lateral nonuniformities is much less satisfactory. A study of the a-c conductance of MOS capacitors made by Nicollian and Goetzberger [6] indicated that a conductance measurement can be used to distinguish the effects of lateral nonuniformities from those of interface states. They related the area under the G/ω vs ω curve to the density of interface states and interpreted the broadening of the conductance peak in terms of lateral nonuniformities. Brews and Lopez [9] have proposed two

tests based on a knowledge of the doping profile of the substrate. In one of these the interface potential vs. depletion width is compared with the relationship expected for a uniform structure, and in the other an apparent doping profile is calculated and is compared with the known doping profile. Discrepancies reveal the presence of lateral nonuniformities.

We have developed additional methods for the detection and characterization of lateral nonuniformities [10], and in this paper we discuss two techniques which are based respectively on the frequency dependence and the temperature dependence of the response of interface states.

As our model of a laterally nonuniform MIS capacitor we have taken a parallel combination of noninteracting small capacitors, each of which can be considered to be uniform over a small characteristic area. As Brews [11] has pointed out, this model will not provide an accurate representation for lateral nonuniformities of small dimensions (e.g., individual ions) that are laterally well separated. In addition, Gordon [12] has shown that in the inversion regime the individual elementary capacitors interact at their edges through the minority carriers of the inversion layer. Despite these faults, the parallel-capacitor model is a reasonable first-order representation and has the advantage of being more readily amenable to analysis than the more complex representations.

II. FREQUENCY-DISPERSION TEST

When a C-V stretch-out is caused by interface states, the C-V curves will show a frequency dependence that would not otherwise be present. A lack of such frequency dependence will indicate that the observed stretch-out is caused by lateral nonuniformities.

A. Analysis

A uniform MIS capacitor with no interface states has a C-V relationship that is frequency-independent over a wide range of frequencies. At the low-frequency end, the capacitance becomes frequency-dependent when the minority carriers at the interface are able to follow the a-c signal. In the absence of a source of minority carriers such as a p-n junction or an inverted region at the periphery of the field plate, the response time of minority carriers is comparatively long and the corresponding frequency dependence at room temperature is normally limited to frequencies below 100 Hz. At the high-frequency end the response is limited by the ohmic relaxation time of the bulk, which is given by $\tau_\Omega = \rho\varepsilon$ where ρ is the resistivity of the semiconductor and ε is its dielectric permittivity. For 10 Ω-cm silicon, the corresponding frequency, $f_\Omega = 1/2\pi\tau_\Omega$, is of the order of 10^{10} Hz. We therefore conclude that the room-temperature C-V relationship of a uniform MIS capacitor without interface states should be frequency-independent in the approximate frequency range from 100 Hz to 10^{10} Hz. We can further conclude that, to the extent that a laterally nonuniform MIS capacitor can be modeled as a parallel set of small, noninteracting capacitors, the C-V relationship of a nonuniform capacitor with negligible interface states should also be frequency-independent over the same frequency range.

In contrast with the frequency-independence of lateral nonuniformities, interface states cause the MIS C-V characteristics to be frequency-dependent, particularly in the depletion regime and typically in the frequency range between a few hundred Hz and 1 MHz. Because of the step-function-like property of the Fermi-Dirac function, only those interface states whose energies lie within a few kT of the Fermi energy can contribute appreciably

to the interface-state capacitance. In accumulation and depletion, the communication between these states and the minority carrier band can be neglected. If we assume that the states are located at a sharply defined interface between the insulator and semiconductor and can therefore communicate directly with the majority-carrier band of the semiconductor, Shockley-Read statistics [13] can be used to compute the time constant associated with the electronic activity of the interface states. Assuming electrons to be the majority carriers, the time constant for states at the Fermi level can be expressed as [6], [14]

$$\tau = \frac{1}{2v_{th}\sigma_n n_{sF}} \tag{1}$$

where v_{th} is the thermal velocity of electrons in the semiconductor, σ_n is the capture cross section of the states for electrons, and n_{sF} is the concentration of free electrons at the interface when the Fermi level at the interface coincides with the energy level of the interface states under consideration:

$$n_{sF} = N_c \exp[-(E_c - E_s)/kT] \tag{2}$$

where N_c is the effective density of states in the conduction band, $E_c - E_s$ is the depth of the interface states below the edge of the conduction band, k is Boltzmann's constant, and T is the absolute temperature.

The time constant defines a characteristic frequency for the interface states at the given level:

$$f_c = \frac{1}{2\pi\tau} \tag{3}$$

By use of (1) and (2) this can be written as

$$f_c = \frac{v_{th}\sigma_n N_c}{\pi} \exp[-(E_c - E_s)/kT] \tag{4}$$

for interface states at the energy level E_s.

The interface states at or near the Fermi level will contribute to the capacitance of the MIS structure at frequencies below f_c but will not contribute at frequencies well above f_c. More precise statements can be made for particular interface-state distributions. It can be shown [6], [15] that for a discrete-level state located at the Fermi level, the low-frequency value of the interface-state capacitance is $C_s = q^2 N_s/4kT$ per unit area where q is the electronic charge and N_s is the concentration of states per unit area, and that the equivalent parallel capacitance of the states varies from 90% to 10% of this value as the frequency is varied from $f_c/3$ to $3f_c$. It can also be shown [6],[15] that a continuum of states uniformly distributed in energy has a low-frequency capacitance given by $C_s = qN_{ss}$ per unit area where N_{ss} is the concentration of states per unit area per eV, and that the equivalent parallel capacitance of the states varies from 90% to 10% of this value as the frequency is varied from approximately $0.3f_c$ to $7.5f_c$. Regardless of the distribution in energy of the interface states, at frequencies well below f_c the capacitance of the MIS structure in the depletion regime is made up of the insulator capacitance, C_i, in series with the parallel combination of C_s and the depletion-layer capacitance, C_D, and hence the low-frequency, or quasi-static, capacitance will be given by [6]

$$C_{LF} = [1/C_i + 1/(C_s + C_D)]^{-1} . \qquad (5)$$

At frequencies well above f_c the contribution from the interface states will approach zero and the capacitance will have its high-frequency value:

$$C_{HF} = (1/C_i + 1/C_D)^{-1} . \qquad (6)$$

To obtain an estimate of the characteristic frequencies associated with interface states at different depths, we use (4) with the following typical values for the parameters: $v_{th} = 10^7$ cm/sec, $\sigma_n = 10^{-15}$ cm^2 [6],[16], and $N_c = 3 \times 10^{19}$ cm^{-3}. For room temperature, (4) yields the following values of f_c for different values of the depth $(E_c - E_s)/q$ in the depletion regime: 7.9×10^5 Hz for 0.3 eV, 1.6×10^4 Hz for 0.4 eV, and 3.2×10^2 Hz for 0.5 eV. These frequencies are well within the range of convenient measurement.

In summary, the frequency-dispersion test is as follows: If a C-V stretch-out is frequency-independent in the frequency range from a few hundred Hz to 1 MHz, it is due to lateral nonuniformities. Any frequency dependence in this range is caused by interface states. Furthermore, as has been observed by Castagne and Vapaille [1], the use of different methods for calculating the densities of interface states produces inconsistent results if lateral nonuniformities are present. If frequency dispersion is observed in the C-V characteristics, additional evidence that lateral nonuniformities are not important in creating the stretch-out can be obtained by calculating the interface-state density either from the high-frequency C-V

curve alone [3] or from the low-frequency or quasi-static C-V curve alone [5], [7], [8]. Equations (5) and (6) can then be used to check whether the calculated density of interface states can account entirely for the difference between the high-frequency and low-frequency capacitances in the depletion regime.

B. Examples

The results of two sets of experiments will be given here as examples of the application of the frequency-dispersion method.

Example 1

Figure 1 shows C-V curves taken on an MOS capacitor having an n-type silicon substrate with a resistivity of 1-2 ohm-cm, an HCl-steam grown SiO_2 insulator with a thickness of 2560 Å, and an aluminum field plate. The C-V characteristic of the fresh sample was taken at four different frequencies: 1 kHz, 10 kHz, 100 kHz, and 1 MHz. Substantially identical results, as shown by the dashed curve of Fig. 1, were obtained on the fresh sample at all four frequencies. This curve is nearly ideal in shape and shows a flatband voltage of approximately -0.5 V. The insulator was then subjected to high-field stress by applying -175 V to the field plate for 10 hrs at room temperature (average field in the oxide approximately 6.8 MV/cm). As shown by the solid curves of Fig. 1, the C-V characteristics after this treatment show an appreciable stretch-out and the quasi-static capacitance is considerably greater than the 1-MHz capacitance in the depletion regime. The frequency dispersion shown by the solid curves indicates the existence of interface states that were not present in the fresh sample and which were presumably generated during the high-field treatment. To check whether lateral nonuniformities were also important, we perform the following calculation at Point A in Fig. 1, which corresponds to a surface potential of 0.15 eV as determined by Berglund's method [5]. At this value of surface potential the 1-MHz capacitance should closely approximate the true high-frequency capacitance. The density of interface states was computed by

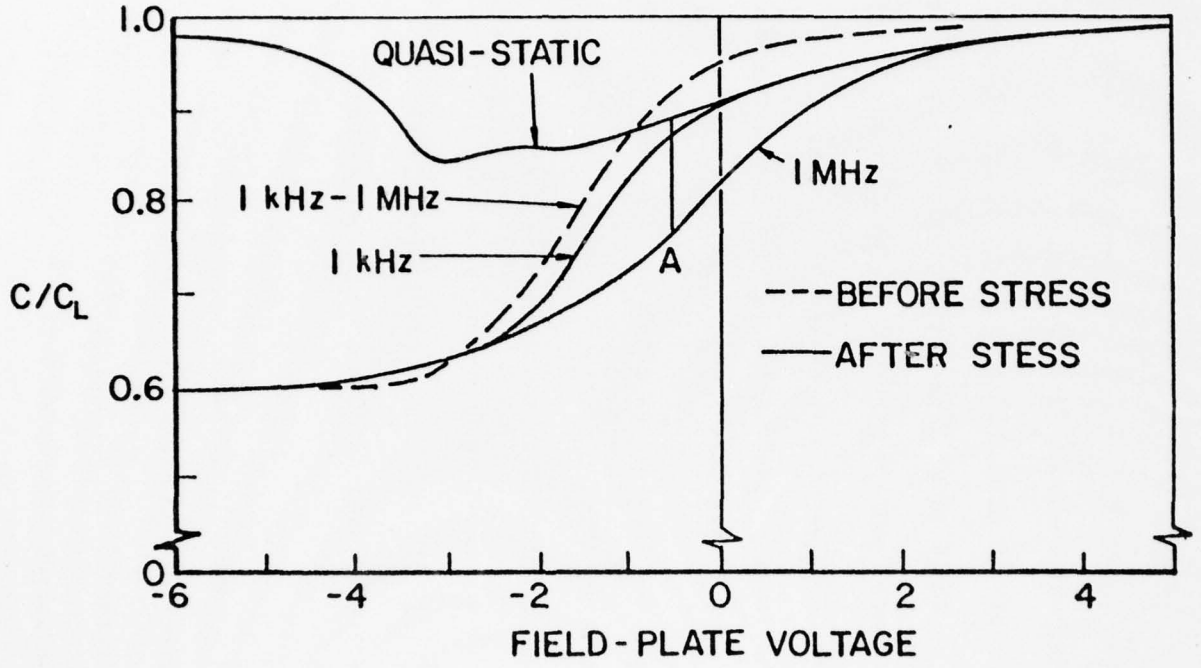

Fig. 1. Room-temperature C-V curves, before and after high-field stress, for the MOS capacitor of Example 1. The frequency dispersion after high-field stress shows the presence of interface states.

Terman's method [3] to be approximately 4.5×10^{11} $cm^{-2}eV^{-1}$ in this portion of the silicon bandgap, giving a low-frequency interface-state capacitance $C_s = qN_{ss} = 7.2 \times 10^{-8}$ F/cm^2. From the known values of C_{HF} and C_i we use (6) to compute C_D at Point A, and then use (5) to compute C_{LF}. This yields $C_{LF}/C_i = 0.90$, which checks with the measured value as shown in Fig. 1. We conclude that the principal cause of stretch-out here is interface states. In Sec. III we shall show by use of a complementary low-temperature test that an identical sample subjected to a similar high-field treatment showed no appreciable lateral nonuniformities.

One final point relating to Fig. 1 deserves mention. Calculation by standard methods [6],[15] based on Shockley-Read statistics indicates that the 1-kHz capacitance at Point A should be essentially equal to the low-frequency value, whereas the actual capacitance is somewhat below this value. A possible explanation is that the interface states are distributed into the insulator so that tunneling is required in addition to Shockley-Read transitions [17]. It has been shown [18] that this effect introduces a time-constant dispersion even for traps at a single level.

Example 2

As a contrasting example we show in Fig. 2 the results obtained on an MOS capacitor in which the stretch-out of the C-V curves was apparently caused by a laterally nonuniform storage of charge in the insulator. The sample had an n-type silicon substrate with a resistivity of 3-5 ohm-cm, an SiO_2 insulator which was thermally grown in dry oxygen to a thickness of 4700 Å, and an aluminum field plate. The sample, with field plate positive, had been bombarded with a 4.5 keV electron beam, after which the

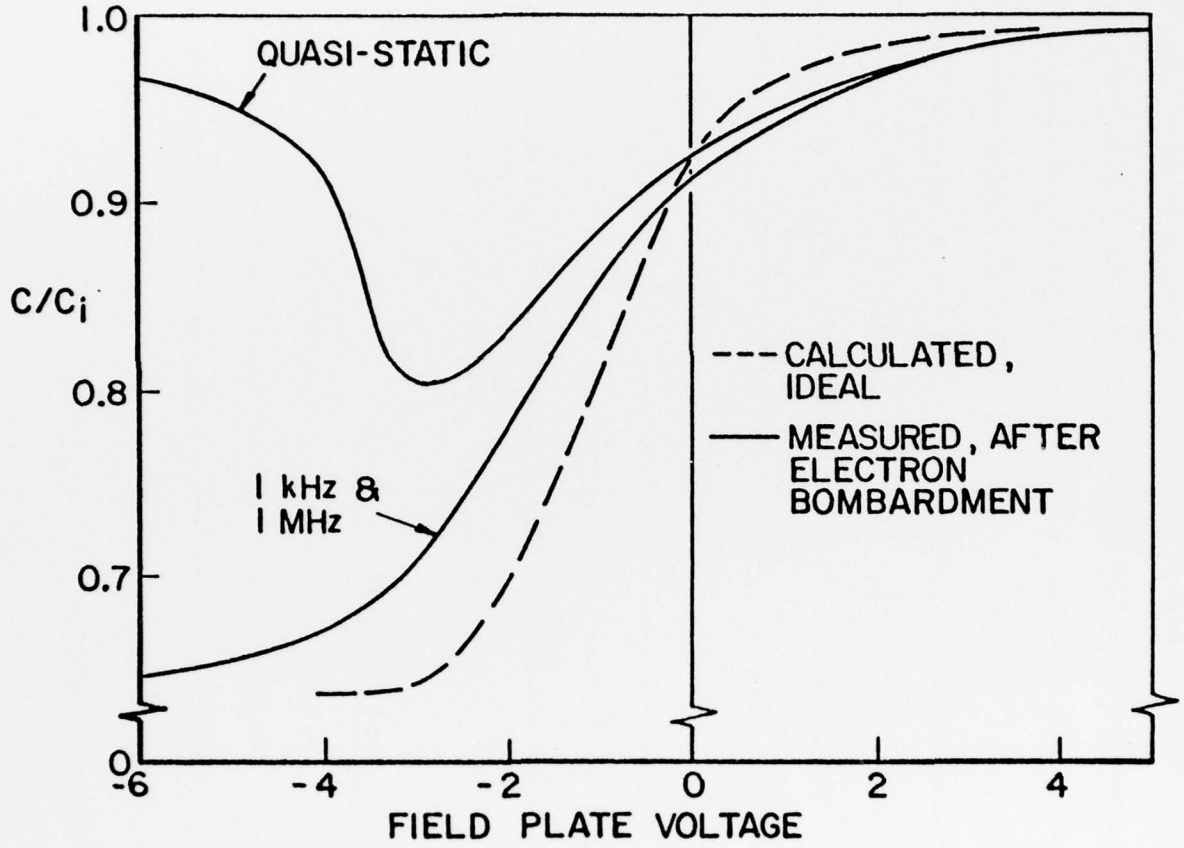

Fig. 2. Room-temperature C-V curves for Example 2. The solid curves were taken after electron bombardment and anneal (see text). The lack of frequency dispersion between 1 kHz and 1 MHz indicates that the stretch-out was caused by lateral nonuniformities.

sample was annealed at 350°C for one hour. The solid curves of Fig. 2 show the quasi-static and high-frequency C-V characteristics of the sample after this treatment. Compared with the calculated ideal high-frequency characteristic, shown dashed in Fig. 2, the measured curves are stretched out, and the quasi-static curve does not coincide with the high-frequency curve in the accumulation and depletion regions. The question of whether the stretch-out was caused by interface states or by lateral nonuniformities was investigated by taking the high-frequency C-V characteristic at two different frequencies: 1 kHz and 1 MHz. This resulted in curves which were essentially identical and which are presented as a single solid curve in Fig. 2. The lack of frequency dispersion indicates that the observed stretch-out was due to lateral nonuniformities. Tests on the electron beam showed that the beam was nonuniform across its cross section, and it seems likely that the charge storage induced in the insulator by the bombardment was laterally nonuniform.

III. LOW-TEMPERATURE TEST

In this section we discuss a method which is based on the principle that, except for states near the band edges, carriers can be frozen into the interface states by reducing the temperature of the sample, whereas reduced temperature will have no similar effect on a C-V stretch-out which is caused by lateral nonuniformities.

A. Analysis

The mean time for emission of a trapped electron from an interface state is given by Shockley-Read statistics as [13]

$$\tau_e = \frac{1}{v_{th} \sigma_n N_c} \exp[(E_c - E_s)/kT], \qquad (7)$$

this being precisely twice the time constant associated with the characteristic frequency and given by (1). We shall assume a temperature of $100^{\circ}K$ and calculate emission times using the following typical values for the parameters: $v_{th} = 6 \times 10^{6}$ cm/sec, $\sigma_n = 10^{-15}$ cm^2, and $N_c = 6 \times 10^{18}$ cm^{-3}. Equation (7) then yields the following values of τ_e for different values of the depth of the interface states: for 10^{-2} sec, 0.17 eV; for 1 sec, 0.21 eV; for 10^{2} sec, 0.25 eV; and for 10^{4} sec, 0.29 eV. At $100^{\circ}K$ the emission time increases by approximately a factor of 10 as the depth of the state is increased by 0.02 eV, and is quite long for states that are more than 0.25 eV from a band edge.

The proposed procedure can be understood with the aid of Fig. 3. The MOS capacitor is cooled to approximately liquid nitrogen temperature and is biased into accumulation to fill the interface states with majority carriers. The C-V characteristic is then taken as the bias is swept toward depletion at a reasonably fast rate so that the entire sweep is accomplished within, say, a few seconds. As the capacitor goes from accumulation into depletion, the interface states within about 0.25 eV from the majority-carrier band will empty rapidly, but majority carriers will be frozen into the deeper states and will provide a fixed charge throughout the remainder of the sweep. If lateral nonuniformities are negligible, the lower part of the C-V curve will coincide with an ideal characteristic which has been translated along the voltage axis. The effect is shown in Fig. 3(a) for a capacitor in which the stretch-out is caused by interface states. At Point A the Fermi level in the substrate has fallen to 0.25 eV below the majority-carrier band edge, and below this point the measured (solid) curve coincides with the

translated ideal (dashed) curve. If, as in Fig. 3(b), the C-V stretch-out is due to lateral nonuniformities, the measured low-temperature curve will remain stretched out and cannot be made to coincide with the ideal characteristic below Point A.

An additional test, based on an observation originally made by Goetzberger and Irwin [19], is also illustrated in Fig. 3. After the sweep into deep depletion has been completed (Point B), temporary illumination of the capacitor with bandgap light will provide minority carriers - holes, in this example - to the interface and will bring the capacitor out of deep depletion (Point C). The interface states will now capture holes and will go into their more positive charge condition. If the bias is then swept toward accumulation, the holes will be ejected from the interface and will move into the bulk [19], whereupon the states within about 0.25 eV from the edge of the valence band will be able to emit holes into the valence band and will go into their more negative charge condition. States above this, however, will have long hole-emission times and will remain temporarily in their more positive condition. As the bands continue to straighten, the density of free electrons will eventually increase to the point where the electron capture time becomes smaller than the sweep time, and the remaining states with energies up to the Fermi level will thereupon all capture electrons. This will occur over a small change of surface potential and will cause a ledge in the C-V characteristic [19] such as is shown between Points D and E in Fig. 3(a). The absence of such a ledge, as in Fig. 3(b), provides evidence that the observed C-V stretch-out is caused by lateral nonuniformities rather than by interface states.

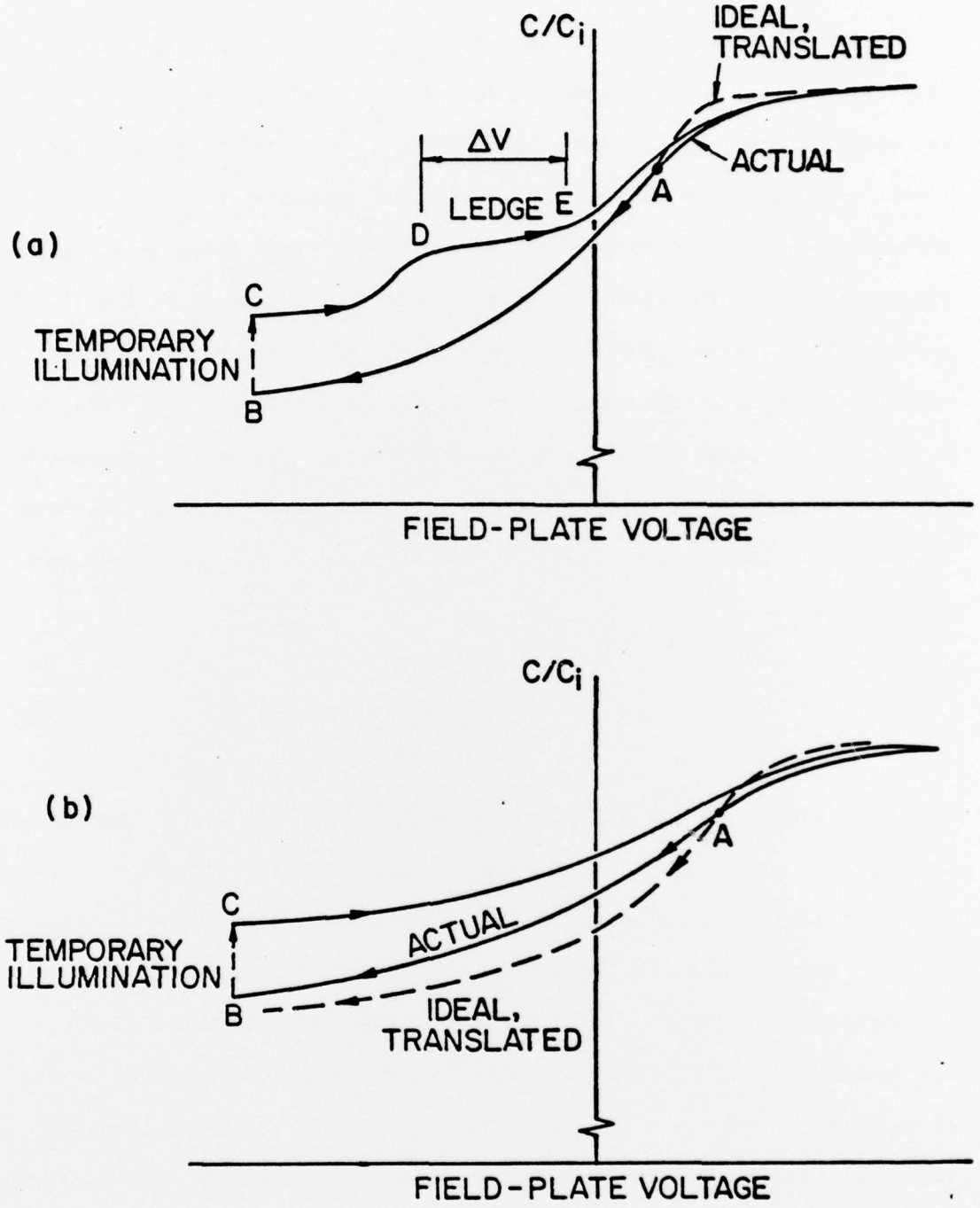

Fig. 3. Low-temperature ($100^{\circ}K$) C-V characteristics of MIS capacitors, shown schematically. (a) Uniform capacitor with interface states. (b) Capacitor with lateral nonuniformities. Point A corresponds to $(E_c - E_F)/q \approx 0.25$ eV on the ideal curve.

When a ledge exists, an approximate value for the density of interface states in the central region of the band gap can be computed from the width of the ledge, shown as ΔV in Fig. 3(a). The states that capture electrons during this time will be those that extend from about 0.25 eV above the valence band up to the position of the Fermi level at which the electron capture time becomes comparable with the sweep time. The electron capture time is given by $\tau_c = 1/v_{th}\sigma_n n_s$ [13], where n_s is the concentration of free electrons at the interface. Since $n_s = N_c \exp[-(E_c - E_F)/kT]$, where $E_c - E_F$ is the depth of the Fermi level below the edge of the conduction band at the interface, we have for the electron capture time of all interface states, regardless of their depth, that are in their more positive charge condition:

$$\tau_c = \frac{1}{v_{th}\sigma_n N_c} \exp[(E_c - E_F)/kT] \qquad (9)$$

The right side of this expression is identical with (7) except that E_F has replaced E_s, and consequently the results computed from (7) can be adapted to our present purpose: When the Fermi level is 0.25 eV below the edge of the conduction band at the interface, the capture time at $100^{\circ}K$ will be approximately 10^2 sec, and the time will change by a factor of 10 for approximately each change of 0.02 eV in the depth of the Fermi level. If we take $(E_c - E_F)/q = 0.25$ eV to be the depth of the Fermi level at which the transition occurs, the energy range of the states that make the transition is approximately $\Delta\phi \approx 1.1 - 2 \times 0.25 = 0.6$ eV for silicon at $100^{\circ}K$. The charge captured by these states is $q\bar{N}_{ss}\Delta\phi$ where $\bar{N}_{ss}$ is the average concentration of states ($cm^{-2}eV^{-1}$) in the central region of the gap. This is

approximately equal to $C_i \Delta V$, where ΔV is the width of the ledge. Thus we have

$$\bar{N}_{ss} \approx \frac{C_i \Delta V}{q \Delta \phi} . \tag{10}$$

Sources of error in this determination of $\bar{N}_{ss}$ are that $\Delta\phi$ can not be precisely defined and ΔV can not be precisely measured. However, the approximate value of $\bar{N}_{ss}$ determined from (10) can be checked for consistency with values of N_{ss} obtained by other methods, for example from the stretch-out of the high-frequency C-V curve at room temperature. Better definition of the ledge is obtained if the sweep upward is not too fast. A bias sweep that occupies a total of 10^2 - 10^3 sec is generally satisfactory.

B. Examples

Example 3

As the first example of this section we present the results of a low-temperature test on a sample similar to the one used in obtaining the results of Example 1, where the frequency test indicated that the C-V stretch-out observed after high-field stress was caused by interface states rather than by a laterally nonuniform storage of charge. Here we show supporting evidence for that conclusion by use of the low-temperature test on an identical sample which was stressed at -175 V for 6 hrs at room temperature. After stressing, the sample was cooled to 100°K and C-V curves were taken at a frequency of 1 MHz. The lower curve of Fig. 4 is the C-V characteristic of the stressed sample taken by sweeping from accumulation into deep depletion at a rate of 5 V/sec. The dashed curve is the characteristic taken on the sample before high-field stressing and translated to the right by 3.0 V.

The pre-stress curve is essentially ideal in shape, and coincides with the post-stress curve below Point A, which is the point where the Fermi level is approximately 0.25 eV below the conduction band edge. This coincidence indicates that lateral nonuniformities are negligible. As an additional test, the sample was temporarily illuminated with incandescent light, after which the bias was swept from inversion into accumulation at a rate of 5 mV/sec. The result was the upper curve of Fig. 4, which shows an interface-state ledge approximately 2.5 V in width. From (10), using $C_i = 1.33 \times 10^{-8}$ F/cm^2, $\Delta V = 2.5$ V, and $\Delta\phi = 0.6$ V, we compute $\bar{N}_{ss} \approx 3.5 \times 10^{11}$ cm^{-2} eV^{-1} in the central region of the band gap. This figure agrees very well with the results obtained from the room-temperature high-frequency characteristic by Terman's method [3], which indicated interface-state densities ranging from 3.0×10^{11} cm^{-2} eV^{-1} at midgap to 4.5×10^{11} cm^{-2}eV^{-1} at 0.2 eV above midgap. We conclude that the C-V stretch-out which appeared as the result of negative-field-plate high-field stress was caused by interface states that were generated during the stressing, and that lateral nonuniformities were not an important factor in the stretch-out.

Example 4

As the second example of this section we show the results obtained on an MOS capacitor in which C-V stretch-out was induced in a sodium-contaminated sample by a bias-temperature stress treatment in which the sample was heated to 160°C for 1 hr with the field plate positive. The sample had an n-type (100) silicon substrate with a resistivity of 3-5 ohm-cm and a 3500-Å HCl-steam grown oxide. The solid curve of Fig. 5 is the 1-MHz C-V characteristic of the stressed sample taken at a temperature of 100°K

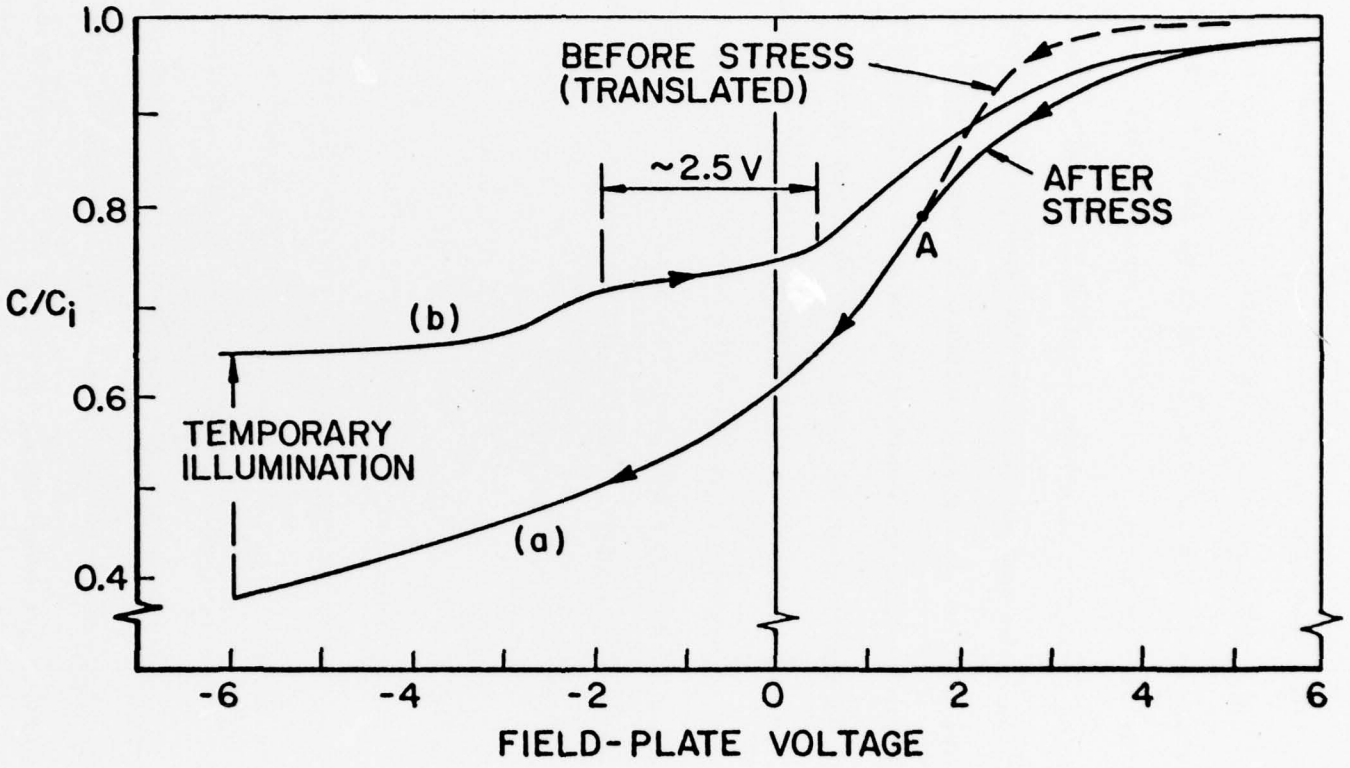

Fig. 4. For example 3. Low-temperature (100°K), high-frequency (1 MHz) C-V characteristics of an MOS capacitor after high-field stress. Curve (a): Downward sweep at 5 V/sec. Coincidence with the translated pre-stress curve below Point A indicates that lateral nonuniformities are negligible. Curve (b): Upward sweep at 5 mV/sec. Ledge shows the presence of interface states.

by sweeping the bias from accumulation into deep depletion at a rate of 5 V/sec. The dashed curve is the similar characteristic taken on the same sample before stressing and translated along the voltage axis by -21 V to make the two curves coincide at Point A, which is the point where the Fermi level at the interface is approximately 0.25 eV below the edge of the conduction band. The dashed curve for the fresh sample is essentially ideal in shape. The lack of coincidence between the two curves indicates that the stressed sample possesses substantial lateral nonuniformities, presumably a nonuniform distribution of sodium ions near the interface. This result agrees with the observations of DiStephano [20] and of Williams and Woods [21], who used scanning internal-photoemission techniques to examine the distribution of positive ions near the interfaces of similarly stressed, sodium-contaminated samples, and found a pronounced nonuniformity in the ionic charge.

IV. SUMMARY

We have discussed here two methods for distinguishing between C-V stretch-out caused by interface states and the very similar stretch-out caused by lateral nonuniformities. The first method is based on the frequency dependence of interface-state capacitance in the depletion region, as contrasted with the frequency independence of the "high-frequency" C-V curves in depletion when the stretch-out is caused by lateral nonuniformities. The difference can be revealed by taking the "high-frequency" curves at two widely separated frequencies, say 1 kHz and 1 MHz. The difference between the true high-frequency capacitance and the quasi-static capacitance in

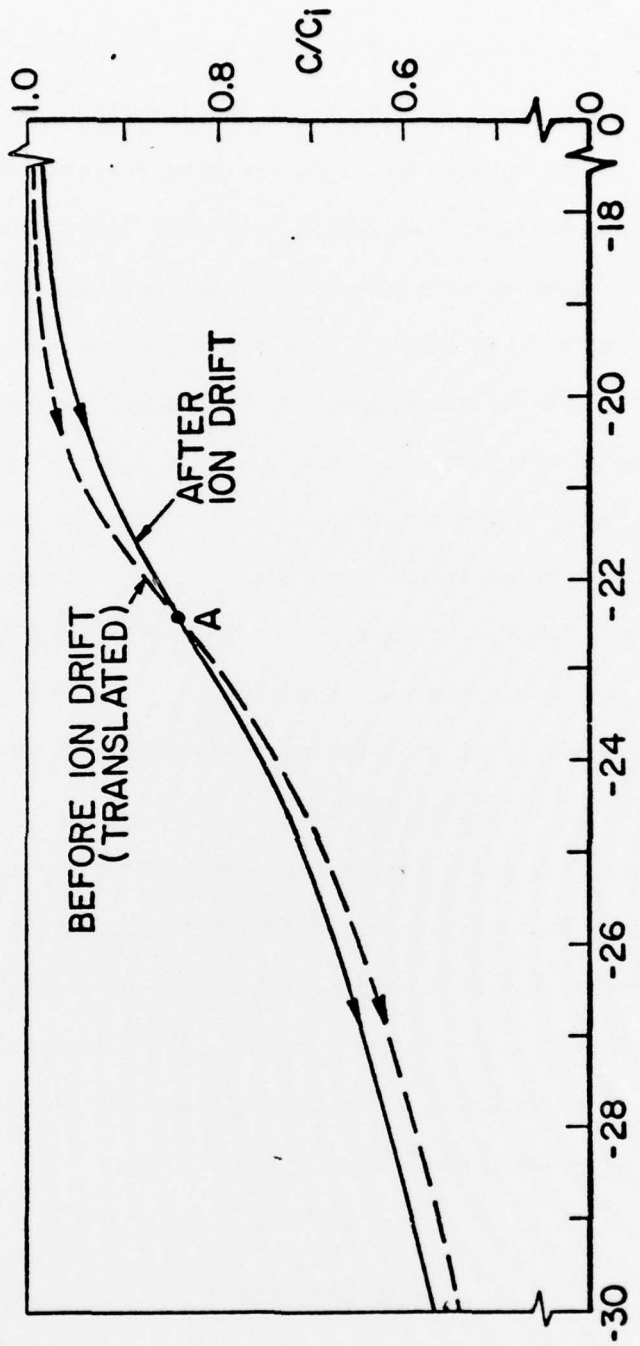

Fig. 5. For Example 4. Low-temperature (100°K), high-frequency (1 MHz) C-V characteristics. Solid curve: After drift of sodium ions to the Si-SiO_2 interface. Dashed curve: Before ion drift, curve translated by -21 V. Lack of coincidence below Point A shows the presence of lateral nonuniformities.

depletion can, in the absence of lateral nonuniformities, be accounted for entirely by the frequency dependence of the interface-state capacitance.

The second method relies on freezing the carriers into interface states at low temperatures, say 100°K. At this temperature the carriers in states deeper than about 0.25 eV from the band edge will be frozen into the states for sufficient time to take a C-V characteristic. The suggested procedure is to cool the MIS capacitor, bias the structure into accumulation to fill the states with majority carriers, and take a high-frequency C-V curve while sweeping rapidly into deep depletion. The shape of this curve is then compared with an ideal (translated) curve. A lack of correspondence between the curves indicates that C-V stretch-out is caused by lateral nonuniformities. Correspondence in the region where the Fermi level is further than about 0.25 eV from the majority-carrier band edge indicates that the C-V stretch-out is caused by interface states.

An auxiliary low-temperature test is provided by temporarily illuminating the MIS structure after the sweep into depletion, following which a slow sweep is made toward accumulation. A ledge in the characteristic will indicate the presence of interface states in the central region of the band gap. The concentration of interface states in the central portion of the bandgap can be obtained by use of (10).

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